METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION DUE TO GATE LEAKAGE DURING SLEEP MODE

ABSTRACT

[0035] One embodiment of the present invention provides a system that achieves low gate leakage current in an integrated circuit during sleep mode. Upon entering sleep mode, the system reduces the power supply voltage applied to the integrated circuit to a low voltage level, wherein the low voltage level is low enough to provide a low gate leakage current, but is high enough to maintain state in the integrated circuit.